	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	16	(retrograde with implantation) and semiconductor and 438/301,407,705,738,526,282,514.ccls.	USPAT; US-PGPUB	2002/01/24 14:23			0
2	BRS	L4	20	(hard adj mask) and (low adj k adj dielectric)and 438/637,700.ccls.	USPAT	2002/01/24 14:27			0

	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	5	(retrograde adj implantation) and semiconductor	USPAT; US-PGPUB	2002/01/23 10:55
2	BRS	15	(retrograde with implantation) and semiconductor	EPO; JPO; DERWENT; IBM_TDB	2002/01/23 10:41
3	BRS	122	(retrograde with implantation) and semiconductor	USPAT; US-PGPUB	2002/01/23 15:57
4	BRS	3	(retrograde with implantation with (dielectric or insulator)) and semiconductor	USPAT; US-PGPUB	2002/01/23 12:22
5	BRS	0	(retrograde with implantation with (dielectric or insulator)) and semiconductor	EPO; JPO; DERWENT; IBM_TDB	2002/01/23 12:21
6	BRS	76	(retrograde with implantation) and semiconductor and (via or trench)	USPAT; US-PGPUB	2002/01/23 12:34
7	BRS	569	((multiple or plurality) with implantation) and semiconductor and (via or trench)	USPAT; US-PGPUB	2002/01/23 12:40
8	BRS	558	(((multiple or plurality) with implantation) and semiconductor and (via or trench)) not ((retrograde with implantation) and semiconductor and (via or trench))	USPAT; US-PGPUB	2002/01/23 12:41
9	BRS	1	"5817580".PN.	USPAT	2002/01/23 14:30
10	BRS	1	"4652234".PN.	USPAT	2002/01/23 14:31
11	BRS	40	(retrograde near3 implantation) and semiconductor	USPAT; US-PGPUB	2002/01/23 15:58
12	BRS	32	((retrograde near3 implantation) and semiconductor) and energy	USPAT; US-PGPUB	2002/01/23 16:01
13	BRS	26	(((retrograde near3 implantation) and semiconductor) and energy) and (three or third)	USPAT; US-PGPUB	2002/01/24 10:14
14	BRS	2	(hard adj mask) and (dual adj damascence) and (low adj k adj dielectric)	USPAT	2002/01/24 11:25

	Type	Hits	Search Text	DBs	Time Stamp
15	IS&R	1	("4633289").PN.	USPAT	2002/01/24 10:15
16	BRS	3	(hard adj mask) with dielectric and (dual adj damascence)	USPAT	2002/01/24 11:27
17	BRS	2	((hard adj mask) with dielectric and (low adj k)) and damascence	USPAT	2002/01/24 11:28
18	BRS	61	(hard adj mask) with dielectric and (low adj k)	USPAT	2002/01/24 12:15
19	BRS	61	(hard adj mask) with dielectric and (low adj k)	USPAT	2002/01/24 12:15

DOCUMENT-IDENTIFIER: US 6207517 B1
TITLE: Method of fabricating a semiconductor insulation layer and a
semiconductor component containing the semiconductor insulation layer

---------- KWIC ---------

DEPR:
As shown in FIGS. 3d and 3e, which correspond to FIGS. 3b and 3c in a later
process stage, the method furthermore effects the formation of a respective
p-type and n-type field-effect transistor with a p.sup.- -type channel well
zone 540a and an n.sup.- -type channel well zone 540b in the respective square
zone in accordance with a third mask 311, 312, a superior gate insulator layer
500 and n+/p.sup.+ -type source and drain zones 600a,b and 650a,b,
respectively, in the adjoining region of the semiconductor substrate 10. This
is done by known **implantation** processes and/or **retrograde** well processes.

Also, the retrograde impurity region 130 and the amorphous region 120 function as a channel stop by suppressing diffusion of the displaced atoms and holes from source/drain regions, providing semiconductor devices with improved short channel characteristics.

DOCUMENT-IDENTIFIER: US 6245618 B1
TITLE: Mosfet with localized amorphous region with **retrograde implantation**

---------- KWIC ---------

TTL:
Mosfet with localized amorphous region with **retrograde implantation**

DEPR:
Retrograde impurity region 130 is then formed under the main surface of semiconductor substrate 50 to achieve a gradually increasing impurity concentration under the main surface of the semiconductor substrate 50, as illustrated in FIG. 13. The retrograde impurity region 130 has an impurity concentration peak within the confines of the amorphous region 120. In this embodiment, the retrograde impurity region 130 is formed by ion implanting a p type impurity, as shown by arrows D, employing the dielectric layer 90 and sidewall spacers 70 as a mask, to achieve a gradually increasing impurity concentration in the semiconductor substrate 50 below the temporary gate oxide 52. Such a method of forming a gradually increasing impurity concentration, known as a retrograde well or **retrograde implantation**, is conventionally achieved by ion implanting impurity ions with a high energy into a semiconductor substrate, for example, as disclosed in John Yuan-Tai Chen, "Quadruple-well CMOS for VLSI technology," IEEE Transactions on Electron Devices, vol. ED-31, No. 7, July 1984 and U.S. Pat. No. 4,633,289. The retrograde impurity region 130 reduces the resistance against the latch-up phenomenon, thereby improving the transistor's reliability.

DOCUMENT-IDENTIFIER: US 6207576 B1
TITLE: Self-aligned dual damascene arrangement for metal interconnection with
low k dielectric constant materials and oxide etch stop layer

---------- KWIC ---------

TTL:
Self-aligned dual damascene arrangement for metal interconnection with **low k**
dielectric constant materials and oxide etch stop layer

ABPL:
A method of forming a self-aligned dual damascene structure in a semiconductor
device arrangement forms a first **low k** dielectric material over an underlying
metal interconnect layer, such as a copper interconnect layer. An oxide etch
stop layer is formed on the first **low k** dielectric layer, and a second **low k**
dielectric layer is formed on the oxide etch stop layer. A trench is etched
into the second **low k** dielectric layer, followed by the etching of a via into
the first **low k** dielectric layer. The first and second **low k** dielectric
materials are different from one another so that they have different
sensitivity to at least one etchant chemistry. Undercutting in the second
dielectric layer caused by overetching is thereby prevented during the etching
of the via in the second dielectric layer by employing an etch chemistry that
etches only the first **low k** dielectric material and not the second **low k**
dielectric material.

BSPR:
In the formation of a dual damascene structure in a self-aligned manner, a
conductive line and vias that connect the line to

conductive elements in a previously formed underlying conductive interconnect layer, are simultaneously deposited. The conductive material is deposited into openings (e.g., via holes and trenches) created in dielectric material that overlays the conductive interconnect layer. Typically, a first layer of dielectric material is deposited over a bottom etch stop layer that covers and protects the conductive interconnect layer. A middle etch stop layer is then deposited over the first dielectric layer. A pattern is then etched into the middle stop layer to define the feature, such as a via hole, that will later be etched into the first dielectric layer. Once the middle etch stop layer is patterned, a second dielectric layer is deposited on the middle etch stop layer. A **hard mask** layer may then be deposited on the second **dielectric** layer. A desired feature, such as a trench, is etched through the **hard mask** layer and the second **dielectric** layer. This etching continues so that the first dielectric layer is etched in the same step as the second dielectric layer. The etching of the two dielectric layers in a single etching step reduces the number of manufacturing steps. The bottom etch stop layer within the via hole, which has protected the conductive material in the conductive interconnect layer, is then removed with a different etchant chemistry. With the via holes now formed in the first dielectric layer and a trench formed in the second dielectric layer, conductive material is simultaneously deposited in the via and the trench in a single deposition step. (If copper is used as the conductive material, a barrier layer is conventionally deposited first, to prevent copper diffusion.) The conductive material makes electrically conductive contact with the conductive

material in the underlying conductive interconnect layer.

BSPR:
In efforts to improve the operating performance of a chip, **low k** dielectric materials have been increasingly investigated for use as replacements for dielectric materials with higher k values. Lowering the overall k values of the dielectric layers employed in the metal interconnect layers lowers the RC of the chip and improves its performance. However, **low k** materials, such as benzocyclobutene (BCB), hydrogen silsesquioxane (HSQ), SiOF, and the material sold under the trade name of FLARE, are often more difficult to handle than traditionally employed higher k materials, such as an oxide.

BSPR:
When forming a dual damascene structure in a self-aligned manner in which a **low k** dielectric material, such as BCB, is substituted for higher k dielectric materials in the two dielectric layers in which the vias and the trench are created, the problem of "undercutting" becomes a concern. Undercutting is the undesired enlargement of one of the holes created in one of the dielectric layers. As seen in FIG. 1 which depicts a cross-section of an interconnect region processed in accordance with the prior art, a trench dielectric layer 16 is overetched during the etching of the trench dielectric layer 16 and a via dielectric layer 12. (The middle etch stop layer 14 was previously etched prior to the deposition of the second **dielectric** layer 16.) An undercut appears below a **hard mask** layer 18 and is due to the overetching. The overetching typically occurs to assure adequate etching of the via dielectric layer 12 down to a bottom etch stop layer 12 that overlays the conductive layer 10. The

undercutting causes the ultimately formed via structure to be incorrectly
shaped and presents a critical dimension control problem in a **low k** etching
process.

BSPR:
There is a need for a method and arrangement that provides a film with a lower
overall dielectric constant value that will exhibit improved overall
performance, yet avoids the undercutting that occurs with the use of a **low k**
dielectric material in the dielectric layers of a dual damascene interconnect
arrangement.

BSPR:
This and other needs are met by the present invention which provides a method
of forming an opening in dielectric interconnect layers in a self-aligned
manner by forming a first dielectric layer over a conductive layer. The first
dielectric layer comprises a first **low k** dielectric material. An oxide layer
is formed on the first dielectric layer and patterned to define a first
dielectric layer opening pattern. A second dielectric layer is formed on the
oxide layer. The second dielectric layer comprises a second **low k** dielectric
material having different etch sensitivity than the first **low k** dielectric
material to at least one etchant chemistry. A first opening is etched through
the second dielectric layer. A second opening is then etched through the first
dielectric layer opening pattern in the oxide layer and through the first
dielectric layer, the second opening at least partially overlapping the first
opening.

BSPR:
The use of different **low k** materials in the respective dielectric layers of a

dual damascene arrangement that are selected to have different etch sensitivity to at least one etchant chemistry, in accordance with embodiments of the present invention, allows one dielectric layer to be etched without etching and undercutting the other dielectric layer during a self-aligned dual damascene formation process. The use of an etch stop layer between the first and second dielectric layers, instead of a nitride layer, reduces the overall k value of the arrangement,, since oxide has a lower k value than nitride. To permit an oxide to be used as an etch stop layer, the **low k** dielectric materials may be polymer based, rather than silicon dioxide based. This selection of **low k** materials provides better etch selectivity.

DRPR:
FIG. 3 is a cross-section of the metal interconnect portion of FIG. 2 after a first **low k** dielectric layer is formed on the first etch stop layer, in accordance with embodiments of the present invention.

DRPR:
FIG. 4 is a cross-section of the metal interconnect portion of FIG. 3 following deposition of a second etch stop layer, on the first **low k** dielectric layer, in accordance with embodiments of the present invention.

DRPR:
FIG. 7 is a cross-section of the portion of FIG. 6 following the formation of a second **low k** dielectric layer on the second etch stop layer, in accordance with embodiments of the present invention.

DRPR:
FIG. 8 is a cross-section of the portion of FIG. 7, following the deposition of a **hard mask** layer on the second **low k dielectric** layer, in accordance with embodiments of the present invention.

DRPR:
FIG. 9 is a cross-section of the portion of FIG. 8, following the positioning and patterning of a photoresist layer on the second **low k** dielectric layer to define a first feature to be etched in the second **low k** dielectric layer, in accordance with embodiments of the present invention.

DRPR:
FIG. 10 is a cross-section of the portion of FIG. 9, after etching through the **hard mask** layer and the second **low k dielectric** layer in accordance with the pattern in the photoresist layer to create a first feature in the second **low k dielectric** layer, in accordance with embodiments of the present invention.

DEPR:
The present invention solves problems associated with the use of **low k** dielectric materials in the dielectric layers of a self-aligned dual damascene arrangement in a metal interconnect region of a semiconductor chip. Specifically, the present invention lowers the overall dielectric constant value of the film and avoids undercutting in the second, upper dielectric layer by providing different **low k** dielectric materials in the two respective dielectric layers in a dual damascene arrangement. The different **low k** dielectric materials are selected so as to have different sensitivity to at least one etchant chemistry. This allows the second feature, such as a via, to be etched into the first dielectric layer without simultaneously overetching and thereby undercutting the second dielectric layer.

DEPR:
As shown in FIG. 3, a first dielectric layer 24 is then formed on the first etch stop layer 22. The dielectric material in the first

dielectric layer 24 is a **low k** (i.e., k<4) dielectric material. The **low k** dielectric material is spin-coated on the first dielectric layer 24 in certain embodiments. A number of different **low k** dielectric materials may be used to form the first dielectric layer 24. However, in the present invention, the **low k** material should not be a silicon dioxide based **low k** dielectric material, such as hydrogen silsesquioxane (HSQ) or SiOF. Silicon dioxide based **low k** dielectric material does not have a suitable etch selectivity with respect to an oxide stop layer. Accordingly, in preferred embodiments of the invention, the **low k** dielectric material is a polymer based material, such as benzocyclobutene (BCB) or FLARE, which is a trademark .TM. of Allied Signal for a **low k** polymer synthesized from perflourobiphenyl with aromatic bisphenols.

DEPR:
The **low k** dielectric material may be formed to a desired thickness, depending on the application required. For purposes of example, assume that the dielectric layer 24 is formed to a thickness of between about 4000 and about 8000 .ANG..

DEPR:
FIG. 7 is a cross-section of the portion of FIG. 6 following the formation of a second dielectric layer 30 over the second etch stop layer 26. In preferred embodiments of the present invention, the second dielectric layer 30 comprises a **low k** dielectric material that is spin-coated on the second etch stop layer 26. Like the **low k** dielectric material in the first dielectric layer 24, the material is the second dielectric layer 30 is a polymer based **low k** dielectric material. However, in order to avoid undercutting of the

low k dielectric material in the second dielectric layer 30, the **low k** dielectric material in the second dielectric layer 30 needs to have a different sensitivity than the **low k** dielectric material in the first dielectric layer 24 to at least one etchant chemistry. This allows the first dielectric layer 24 to be etched while preventing overetching of the second dielectric layer 30.

DEPR:
In the exemplary described embodiment, a suitable polymer based **low k** dielectric material for the first dielectric layer 24 is FLARE, and a suitable polymer based **low k** dielectric material for the second dielectric layer 30 is BCB. As will be described later, these two materials can be etched with different etch chemistries so as to avoid undercutting in the second dielectric layer 30 when only the first dielectric layer 24 is to be etched. The advantages of providing different types of **low k** dielectric materials in the two dielectric layers 24, 30 will become more apparent during the later discussion of the etching steps.

DEPR:
Following the formation of the second **dielectric** layer 30, a **hard mask** layer 32 is deposited on the second **dielectric** layer 30, as depicted in FIG. 8. The **hard mask** layer may comprise silicon nitride, for example, and serves to selectively protect the second **dielectric** layer 30 during the etching steps.

DEPR:
The desired feature, such as a trench opening (a "first" opening), is created (FIG. 10) by etching the **hard mask** layer 32 and the second **dielectric** layer 30. The etching stops at the second etch stop layer 26. A

first etchant recipe may be employed that etches both the **hard mask** layer 32 and the second **dielectric** layer 30. However, in preferred embodiments of the invention, multiple etching steps are used to create the structure depicted in FIG. 10. These include etching the **hard mask** layer 32, followed by etching the second **dielectric** layer 30. The photoresist layer 34 is typically removed by the etching process. If not, a photoresist layer removal step can be performed.

DEPR:
As depicted in FIG. 11, the first dielectric layer 24 is now etched to create the second opening, such as a via hole. It is undesirable to etch the second dielectric layer 30 any further during this step, as it creates a problem in critical dimension control. See, for example, the overetching of the second dielectric layer depicted in FIG. 1. Further etching of the second **dielectric** layer 30 is only partially prevented by the **hard mask** layer 32. Etching of the second **dielectric** layer 30 in an undercutting fashion that would not be prevented by the **hard mask** layer 32 is nonetheless avoided by the use of an etchant chemistry that does not significantly etch the **low k dielectric** material in the second **dielectric** layer 30, such as described above.

DEPR:
The via hole 36 and the trench 38 are now filled in a simultaneous deposition step with conductive material, preferably copper in certain embodiments of the present invention. The deposition of a barrier layer, typically employed to prevent copper diffusion, is not depicted in order not to obscure the invention. Also, in certain embodiments of the invention, a barrier layer is not needed as certain **low k** dielectric materials form a

self-barrier against
copper diffusion. After chemical mechanical planarization (CMP), the dual
damascene structure of FIG. 13 is formed, having a via (or stud) 40
electrically connecting the underlying conductive layer 20 to a conductive line
42 formed in the trench 38.

DEPR:
The use of different types of **low k** dielectric materials that exhibit different
sensitivity to at least one etchant chemistry, permits the use of **low k**
dielectric materials in the multiple layers of a dual damascene arrangement,
while avoiding the concern of undercutting in one of the dielectric layers.
This use of **low k** dielectric materials provides a chip with lower overall RC
and therefore an improved operating speed. The provision of an oxide etch stop
layer further reduces the overall k value of the chip, and may be employed when
the **low k** dielectric materials are appropriate chosen to be polymer based
instead of silicon dioxide based.

CLPR:
2. The method of claim 1, wherein the first **low k** dielectric material and the
second **low k** dielectric material are polymer based dielectric materials.

CLPR:
3. The method of claim 2, wherein the first and second **low k** dielectric
materials are selected from one of benzocyclobutene (BCB) and a **low k** polymer
synthesized from perflourobiphenyl with aromatic bisphenols.

CLPR:
4. The method of claim 3, wherein the first **low k** dielectric material is
benzocyclobutene and the second **low k** dielectric material is a **low k** polymer

synthesized from perflourobiphenyl with aromatic bisphenols.

CLPR:
5. The method of claim 3, wherein the first **low k** dielectric material is a **low k** polymer synthesized from perflourobinphenyl with aromatic bisphenols and the second **low k** dielectric material is benzocyclobutene.

CLPR:
11. The method of claim 10, wherein the first **low k** dielectric material and the second **low k** dielectric material are polymer dielectric materials.

CLPR:
12. The method of claim 10, further comprising forming a **hard mask** layer on the second **dielectric** layer prior to etching the first and second openings.

CLPR:
13. The method of claim 12, wherein etching the first opening includes creating a second **dielectric** layer opening pattern in the **hard mask** layer and etching the first opening through the second **dielectric** layer in accordance with the second **dielectric** opening pattern in the **hard mask** layer.

CLPV:
forming a first dielectric layer over a conductive layer, the first dielectric layer comprising a first **low k** dielectric material;

CLPV:
forming a second dielectric layer on the oxide layer, the second dielectric layer comprising a second **low k** dielectric material having different etch sensitivity than the first **low k** dielectric material to at least one etchant chemistry;

CLPV:
forming a **hard mask** layer on the second **dielectric** layer and creating a second
dielectric layer opening pattern in the **hard mask** layer,

CLPV:
etching a first opening in the second **dielectric** layer in accordance with the
second **dielectric** opening pattern in the **hard mask** layer, wherein the step of
etching the first opening includes using a first etchant chemistry that
substantially etches only the second **dielectric** layer;

CLPV:
forming a first dielectric layer over a conductive layer, the first dielectric
layer comprising a first **low k** dielectric material;

CLPV:
forming a second dielectric layer on the oxide layer, the second dielectric
layer comprising a second **low k** material having different etch sensitivity than
the first **low k** dielectric material to at least one etchant chemistry;

DOCUMENT-IDENTIFIER: US 6127247 A
TITLE: Method of eliminating photoresist outgassing in constructing CMOS
vertically modulated wells by high **energy** ion implantation

---------- KWIC ---------

TTL:
Method of eliminating photoresist outgassing in constructing CMOS vertically
modulated wells by high **energy** ion implantation

BSPR:
The present invention relates to semiconductor manufacturing processes, and
more specifically, to a method of eliminating photoresist outgassing in
constructing CMOS (complementary metal oxide semiconductor) vertically
modulated wells by high **energy** ion implantation.

BSPR:
In CMOS manufacturing processes, well formation is a vital issue with the
downscaling of transistor size. The undesired lateral diffusion in forming
n-wells and p-wells has the effect of reducing packing density. The concept of
the retrograde well was proposed for using high **energy** implants to place the
dopants at the desired depth without further lateral diffusion. The peak of
the implant can be buried at a certain depth within the substrate by adjusting
implanting **energy**. Thus the lateral diffusion problem can be solved and the
packing density of CMOS devices can be raised by forming the retrograde wells.

BSPR:
In addition, the high **energy** ion implantation is increasingly integrated into
leading edge CMOS processes. The high **energy** ion implantation provides a

simpler process in well formation than conventional diffusion processes.

BSPR:
L. M. Rubin et al. disclose that doped buried layers formed by MeV ion implantation are attractive alternatives to expensive epitaxial substrates for controlling latch-up in CMOS devices, in their work "Process Architectures using MeV implanted Blanket Buried Layers for Latch-Up Improvements on Bulk Silicon" (in Proceeding on Ion implantation Technology, p. 13, 1996). Two different process architecture approaches for forming effective buried layers are discussed. With the process simplifications and cost saving characteristics, the high **energy** ion implantation is widely employed in the leading edge CMOS processes. The largest single production application of high **energy implantation is currently the implanting of retrograde** wells which can replace conventional diffused wells. For future process designs, some investigators are looking at MeV implanted buried layers as a replacement for the latch-up suppression capability of epitaxial layers. A comparison between B.L./C.L. process and PAB architecture is addressed in the work.

BSPR:
W. J. Lee et al. illustrated the issue in the paper "Thick PhotoResist Outgassing During MeV Implantation (Mechanism & Impact on Production)" (in Proceeding on Ion implantation Technology, p. 186, 1996). It is disclosed that the generation of an ion beam and its impact into photoresist-masked wafers will have an adverse effect on the vacuum of an MeV ion implanter. They present the mechanism and effects of photoresist outgassing caused by high **energy** ion implantation (250 KeV to 3 MeV). Due to

photoresist outgassing and
its effects, production usable beam current on small process chamber can be
significantly limited. Photoresist outgassing form various implant conditions
are discussed. It is addressed that outgassing in the process chamber must be
examined to minimize errors in dosimetry resulting from pressure increases.

BSPR:
Therefore, for exploiting the benefit of the high **energy** implantation process
without the doping concentration shift issue caused by photoresist outgassing,
a method of eliminating pressure variation during implantation process is
highly needed. A method of eliminating photoresist outgassing in constructing
CMOS vertically modulated wells by high **energy** ion implantation is in demand.

BSPR:
A method of eliminating photoresist outgassing in constructing CMOS vertically
modulated wells by high **energy** ion implantation is disclosed in the present
invention. A masking layer is used during the implantation and the outgassing
issue in the conventional process can be avoided.

DEPR:
The present invention discloses a method of eliminating photoresist outgassing
in constructing CMOS vertically modulated wells by high **energy** ion
implantation. With the formation of a masking layer, the prior art problem of
dose shifting is solved. The high **energy** implantation process can be performed
without photoresist outgassing and pressure variation.

DEPR:
Following the formation of the pad layer 18, a photoresist layer 20 is formed
thereover, as shown in FIG. 4. Portions of the photoresist layer 20 are then

removed to define p-well regions 22, as indicated in the figure. The p-well regions 22 are regions for doping ions to form the p-wells for the CMOS devices. The portions of the photoresist layer 20 are removed to expose the regions. Next, first p-wells 24 are formed in the substrate 10 under the p-well regions 22. In the case, the first p-wells 24 which are served as shallow p-wells can be formed with a first ion implantation process. For forming p-doped regions, ions like boron-containing ions can be implanted in the preferred embodiments. As an example, the first ion implantation is performed with an **energy** of about 100 keV to about 1000 keV to have a dose of about 1E12 atoms/cm.sup.2 to about 1E13 atoms/cm.sup.2.

DEPR:
Referring to FIG. 7, second p-wells 28 are then formed in the substrate 10 at a level below the first p-wells 24. The second p-wells can be formed with a second ion implantation process. In this case, boron-containing ions are implanted to form the p-doped regions which serve as deep p-wells 28. The boron-containing ions are implanted through the masking layer 26, down to the regions 28 below the first p-wells 24 in the substrate 10. Therefore, vertically modulated p-wells can be formed with the combination of the shallow p-wells 24 and the deep p-wells 28. Under the region uncovered by the masking layer 26, the boron-containing ions are implanted deeper under the region for forming n-wells, as shown in the figure. For achieving deep implantation, a high **energy** implantation process can be employed with an **energy** between about 500 keV to about 5 MeV with a dose of about 5E11 atoms/cm.sup.2 to about 1E15 atoms/cm.sup.2.

DEPR:
Next, n-wells 30 are formed in the substrate 10 under regions uncovered by the masking layer 26. The n-wells are formed substantially under the substrate surface and above the second p-wells 28. In the same way, the n-wells 30 can be formed with a **third** ion implantation process and phosphorus-containing ions can be implanted for n-doped regions. The **third** ion implantation is performed with an **energy** of about 200 keV to about 3 MeV to have a dose of about 1E12 atoms/cm.sup.2 to about 5E13 atoms/cm.sup.2. With the shielding of the masking layer 26 over the p-wells, the implanted ions are unable to penetrate down to the substrate 10 and n-wells 30 are formed only under the openings between the masked regions.

DEPR:
Therefore, vertically modulated wells for constructing CMOS devices are formed with the method described above. The masking layer 26 is used for eliminating photoresist outgassing in prior art well formation processes with high **energy** implantation. Thus the vertically modulated and better-structured wells are provided for forming high performance CMOS devices with raised packing density. The latch-up problem of conventional wells formed by a diffusion scheme can be avoided and the substrate with the well formation technology can be used to replace the conventional expensive epitaxial substrates.

CLPR:
7. The method of claim 1, wherein said **third** ion implantation uses phosphorus-containing ions.

CLPR:
12. The method of claim 8, wherein said **third** ion implantation uses phosphorus-containing ions.

CLPV:
forming first p-wells in said substrate under said p-well regions by a first
ion implantation, said first ion implantation is performed with an **energy**
between about 100 keV to about 1000 keV and a dose of about 1E12 atoms/cm.sup.2
to about 1E13 atoms/cm.sup.2 ;

CLPV:
forming a second p-wells in said substrate at a level below said first p-wells
by a second ion implantation, said second ion implantation is performed with an
energy between about 500 keV to about 5 MeV and a dose of about 5E11
atoms/cm.sup.2 to about 1E15 atoms/cm.sup.2 ;

CLPV:
forming n-wells in said substrate under regions uncovered by said masking layer
and above said second p-wells by a **third** ion implantation, said **third** ion
implantation is performed with an **energy** between about 200 keV to about 3 MeV
and a dose of about 1E12 atoms/cm.sup.2 to about 5E13 atoms/cm.sup.2 ;

CLPV:
forming first p-wells in said substrate under said p-well regions by a first
ion implantation, said first ion implantation is performed with an **energy**
between about 100 keV to about 1000 keV and a dose of about 1E12 atoms/cm.sup.2
to about 1E13 atoms/cm.sup.2 ;

CLPV:
forming a second p-wells in said substrate at a level below said first p-wells
by a second ion implantation, said second ion implantation is performed with an
energy between about 500 keV to about 5 MeV and a dose of about 5E11
atoms/cm.sup.2 to about 1E15 atoms/cm.sup.2 ;

CLPV:
forming n-wells in said substrate under regions uncovered by said masking layer
and above said second p-wells by a **third** ion implantation, said **third** ion
implantation is performed with an **energy** between about 200 keV to about 3 MeV
and a dose of about 1E12 atoms/cm.sup.2 to about 5E13 atoms/cm.sup.2 ;